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09/464,298	12/15/1999	PETER T. LARSEN	042390.P7833	7343

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EXAMINER

TRAN, DENISE

ART UNIT

PAPER NUMBER

2186

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Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/464,298

Applicant(s)

LARSEN ET AL

Examiner

Denise Tran

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 13 January 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-23,32-34 and 38-43 is/are pending in the application.
- 4a) Of the above claim(s)    is/are withdrawn from consideration.
- 5) ☐ Claim(s)    is/are allowed.
- 6) ☒ Claim(s) 1-23,32-34 and 38-43 is/are rejected.
- 7) ☐ Claim(s)    is/are objected to.
- 8) ☐ Claim(s)    are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on    is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on    is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No.   .  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s).
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s)    6) ☐ Other:

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### DETAILED ACTION

1. Applicant's election of claims 1-23 and 32-34 in Paper No. 3 is acknowledged.

Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

2. Claims 1-23, 32-34 and newly added claims 38-43 are presented for examination. Claims 24-31 and 35-37 have been cancelled.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 3, 5-6, 8-10 and 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art, the current specification pages 1-4 and figs 1-2, in view of Walukas, US 6,229,737.

As per claims 1 and 32, AAPA teaches a machine readable medium having embodied thereon a computer program being executable by a machine to perform a method of programming a memory (e.g., page 1) comprising: sending a command to a memory device, said command requesting said memory device to enter a program mode (e.g., page 2, lines 10-20); sending a first address to said memory (e.g., page 2,

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lines 15-20); sending a first data to said memory device, said first data to be programmed at said first address (e.g., page 2, lines 15-21); sending a first write signal to said memory device (e.g., page 4, lines 5-10); sending a second data to said memory device (e.g., fig. 2, data of 230, page 4, lines 15-20); and sending a second write signal to said memory (e.g., fig. 2, write enable, page 4, lines 5-10 and 15-20). AAPA does not explicitly show the use of data packets. Walukas show the use of data packet (e.g., col. 4, lines 1-2. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Walukas into the system of AAPA because it would increase data programming speed and efficiency.

As per claims 3 and 33, AAPA teaches sending a confirmation of said command (e.g., page 3 line 20 to page 4, line 1).

As per claim 5, AAPA teaches wherein said memory device is a flash memory (e.g., page 2, lines 10-13).

As per claims 6 and 34, AAPA teaches sending a termination sequence to exit said program mode (e.g., page 4, lines 11- 13; fig. 1, program done?, 140, 150, and 110).

As per claims 8, AAPA teaches wherein said termination sequence comprising: sending a second address to said memory device, wherein second address is different from said first address (e.g., fig.1, els. 150 and 110).

As per claim 9, AAPA and Walukas, do not explicitly show wherein said termination sequence comprises sending a second address to said memory, wherein said second address is the same as said first address. "Official Notice" is taken that

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both the concept and the advantages of providing termination sequence comprising sending a second address to a memory, wherein a second address is the same as a first address are well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include termination sequence comprising sending a second address to a memory, wherein a second address is the same as a first address because it would allow data reliability and availability by retransmitting data.

As per claim 10, AAPA teaches wherein said first address is sent to said memory device as long as said memory device is in program mode (e.g., page 4, lines 5-10).

5. Claims 2, 4, 7, and 11- 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art, the current specification pages 1-4 and figs 1-2, in view of Walukas, with respect to claims 1 and 32, and further in view of James et al., U.S. patent No. 5966723 (hereinafter James).

As per claims 12, AAPA teaches a method of writing data comprising: receiving a command in a memory device, said command requesting said memory device to enter a program mode (e.g., page 2, lines 10-20); receiving a first address in said memory (e.g., page 2, lines 15-20); receiving a first data, said first data to be programmed at said first address (e.g., page 2, lines 15-21); receiving a write signal (e.g., page 4, lines 5-10); programming said first data to said first address (e.g., page 4, lines 5-10); receiving a second data (e.g., fig. 2, data of 230, page 4, lines 14-20); receiving a second write signal (e.g., page 4, lines 5-10 and 14-20); and programming

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said second data at said second address (e.g., page 4, lines 5-10 and 14-20). AAPA does not explicitly show the use of data packets. Walukas show the use of data packet (e.g., col. 4, lines 1-2. It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Walukas into the system of AAPA because it would increase data programming speed and efficiency. AAPA and Walukas do not explicitly show incrementing said first address to a second address, said second address sequential to said first address. James shows incrementing said first address to a second address, said second address sequential to said first address (e.g., col. 9, lines 15-20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of James into the combined system of AAPA and Walukas because it would increase speed, throughput, and flexibility of programming memory device.

As per claims 2 and 13, AAPA and Walukas do not explicitly show said command is a fast program mode command. James shows the use of command is a fast program mode command (e.g., col. 3, lines 39-41; fig. 4, els 113 and 121). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of James into the combined system of AAPA and Walukas because it would increase speed, throughput, and flexibility of programming memory device.

As per claims 14 and 16-17, AAPA teaches sending a confirmation of said command (e.g., page 3 line 20 to page 4, line 1); wherein said memory device is a flash memory (e.g., page 2, lines 10-13); receiving a termination sequence to exit said program mode (e.g., page 4, lines 11- 13; fig. 1, program done?, 140, 150, and 110).

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As per claims 4 and 15, AAPA and Walukas do not explicitly show wherein said first address being a starting address. James shows wherein said first address being a starting address (e.g., fig. 4, el. 115 and col. 9, lines 40-50). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of James into the combined system of AAPA and Walukas because it would increase speed, throughput, and flexibility of programming memory device.

As per claims 7 and 18, AAPA and Walukas do not explicitly show wherein said termination sequence comprises sending/receiving a data packet comprising all 1's to said memory device. James shows wherein said termination sequence comprises sending/receiving a data packet comprising all 1's to said memory device (e.g., fig. 5, el. 175 and col. 13, lines 40-60). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of James into the combined system of AAPA and Walukas because it would increase speed, throughput, and flexibility of programming memory device. AAPA does not explicitly show the use of data packets. Walukas show the use of data packet (e.g., col. 4, lines 1-2. it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Walukas into the system of AAPA because it would increase data programming speed and efficiency.

As per claim 19, AAPA teaches wherein said termination sequence comprising: receiving a new address in said memory device, wherein said new address is different from said first address (e.g., fig.1, els. 150 and 110).

As per claims 20-21, AAPA teaches wherein said command is received in control logic within said memory device (e.g., page 3, lines 19-20); wherein said control logic is a write state machine (e.g., page 2, lines 5-10).

As per claims 22, AAPA and Walukas do not explicitly show wherein said command causes said control logic to program data at sequential addresses in said memory device. James shows wherein a command causes a control logic to program data at sequential addresses in a memory device (e.g., col. 9, lines 15-20). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of James into the combined system of AAPA and Walukas because it would increase speed, throughput, and flexibility of programming memory device.

As per claims 11 and 23, AAPA and Walukas do not explicitly show polling a pin on said memory device to determine a status or sending a status value from within said memory device to an output pin on said memory device. James shows polling a pin on said memory device to determine a status (e.g., col. 8, lines 52-60) or sending a status value from within said memory device to an output pin on said memory device (e.g., col. 8, lines 52-60). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of James into the combined system of AAPA and Walukas because it would increase speed, throughput, and flexibility of programming memory device.



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6. Claims 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art, the current specification pages 1-4 and figs 1-2, in view of in view of James et al., U.S. patent No. 5966723 (hereinafter James).

As per claims 38, AAPA teaches a method comprising: receiving a command to program a first piece of data at a first address (e.g., page 2, lines 10-20); entering into a program mode (e.g., page 2, lines 10-20); programming said first piece of data at said first address in response to a write signal (e.g., page 4, lines 5-10); receiving a second data (e.g., fig. 2, data of 230, page 4, lines 14-20); checking whether termination of said program mode is indicated or if a second piece of data is to be written (e.g., fig. 1, els. program done?, 140, 150, done or 110); and programming said second piece of data at a second address in response to another write signal (e.g., page 4, lines 5-10 and 14-20). AAPA does not explicitly show exiting said program mode if said termination of said program mode is indicated, else incrementing said first address to a second address. James shows exiting said program mode if said termination of said program mode is indicated (e.g., col. 13, lines 40-50), else incrementing said first address to a second address (e.g., col. 14, lines 1-10). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of James into the combined system of AAPA because it would increase speed, throughput, and flexibility of programming memory device.

As per claims 39-40, AAPA teaches receiving a confirmation command prior to entering said program mode (e.g., page 3, line 2 to page 4, line 10); issuing a status

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value to indicate a status for said programming of said first piece of data (e.g., page 2, line 22 to page 3, line 5).

7. Claims 41-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art, the current specification pages 1-4 and figs 1-2, in view of James et al., U.S. patent No. 5966723 (hereinafter James), with respect to claim 38, further in view of Walukas, US 6,229,737.

As per claim 41, AAPA teaches wherein indication said termination comprising receiving an address unequal to said first address and a predefined data (e.g., fig. 1, els 150-110). Walukas show the use of data packet (e.g., col. 4, lines 1-2). it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of Walukas into the system of AAPA because it would increase data programming speed and efficiency.

As per claims 42-43, AAPA does not explicitly show wherein said predefined data packet is comprised of all 1's or all 0's. James shows wherein said predefined data is comprised of all 1's or all 0's (e.g., fig. 5, els. 173, 175 and col. 11, lines 48-49). It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the teaching of James into the system of AAPA because it would increase speed, throughput, and flexibility of programming memory device. AAPA does not explicitly show the use of data packets. Walukas show the use of data packet (e.g., col. 4, lines 1-2). it would have been obvious to one of ordinary skill in the art at the

time the invention was made to apply the teaching of Walukas into the system of AAPA because it would increase data programming speed and efficiency.

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yiu et al. (5778440) is cited to show method for terminating a program upon detecting a predetermined address/data pattern.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Denise Tran whose telephone number is (703) 305-9823. The examiner can normally be reached on Monday, Thursday, and an alternate Wednesday from 8:30 a.m. to 6:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (703) 305-3821. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 7467-239 for Official communications, (703) 746-7240 for Non Official communications, and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Denise Tran



03/19/03